Bias Circuit for LDMOS Amplifiers

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Many hams are converting to solid-state devices for QRO amplifiers. Most of these amplifiers utilize LDMOS transistors – some are capable of legal limit and beyond. The LDMOS transistors require significant bias current for good gain and linearity, which adds up to a fair amount of power: for example, 2 amps at 50 volts, or 100 watts.

The bias current is often set with a constant gate voltage. However, as the device temperature increases, the device temperature coefficient causes the bias current to increase. This can be a problem, especially for high duty-cycle modes like JT-65 or FT-8. One solution might be more cooling with a big ¼ horsepower blower like we used for tubes; another is temperature compensation of the gate voltage to keep the bias current more constant.

Mike found Ampleon Report R_10032 (www.ampleon.com) describing a temperature compensation circuit for the gate bias voltage. To understand the circuit operation, Paul simulated it using LTspice (www.analog.com). We adjusted the component values to standard 5% resistors, then added a PTT relay and a high voltage three-terminal regulator for 50 volt operation. Then we did a PC board layout to build some prototypes and try them out.

The circuit schematic is shown in Figure 1. The temperature is sensed by a small NPN transistor connected to the **C**, **B**, and **E** terminals and mounted on the amplifier pallet close to the LDMOS transistor. Our choice is the common 2N3904 NPN transistor, readily available and well characterized. The flat side is clamped against the pallet with a dab of heatsink compound.

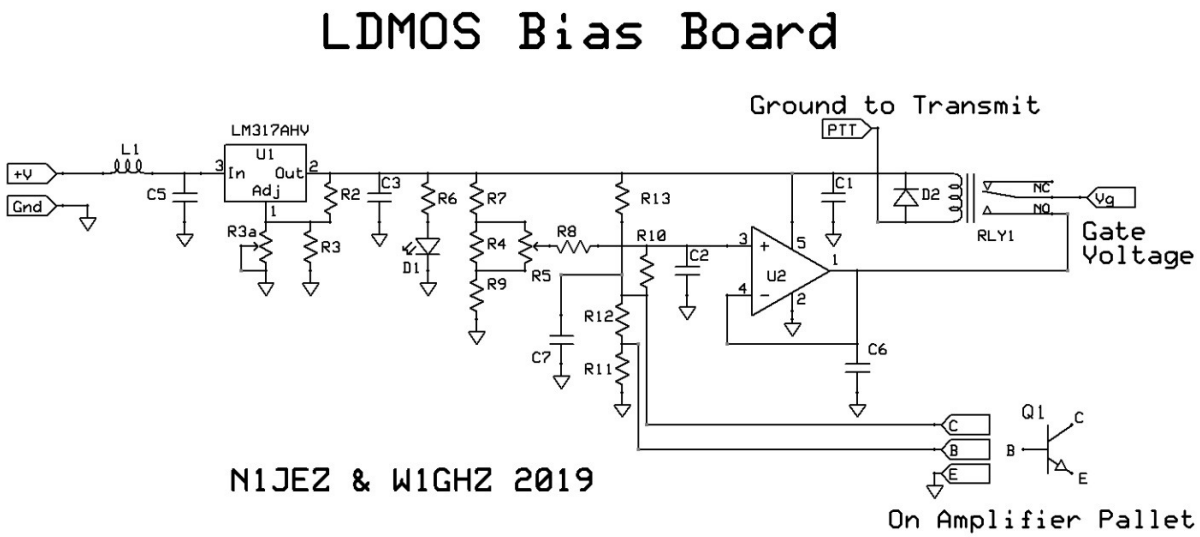

Figure 1 – LDMOS Bias Board Schematic (*see Update at end)*

The gate voltage, and the bias current, is set by the potentiometer R5, which has only a small adjustment range. As the NPN transistor heats up, it draws more collector current which pulls the gate voltage lower (Note: The NPN transistor must be connected – without, the gate voltage is significantly higher). The op-amp, U2, is a unity-gain amplifier to drive the gate. The op-amp was chosen by Ampleon to provide a low output impedance and because it is stable with a capacitive load (like the LDMOS gate).

The other potentiometer, R3a, can be used to set the voltage regulator output voltage. Since this voltage isn't critical, a fixed R3 resistor is adequate – if you are fussy, use the next higher value of R3 and a 100K pot at R3a. The Ampleon circuit set this voltage at 8 volts. Mike had some relays suitable for 8 volts, but Paul only had 12 volt relays so adjusted the bias circuit values for 12 volt operation. Resistor values for both options are in the parts list. The relay may also be powered separately, from terminal VR, after cutting the trace next to C3 at the point marked ✖.

Temperature compensation is set by R10. The 10K value shown is for the nominal -2mv/°C. Reducing the value of R10 will increase the temperature compensation, and vice-versa.

Ampleon suggests an additional resistor, 5 to 20 ohms, in series with the LDMOS gate to ensure low-frequency stability. Adding a 5 volt Zener diode to ground might help protect the sensitive LDMOS gate from voltage and static spikes.

Figure 2 shows a prototype PC board mounted on an amplifier. Construction might be more elegant if it weren't an add-on.

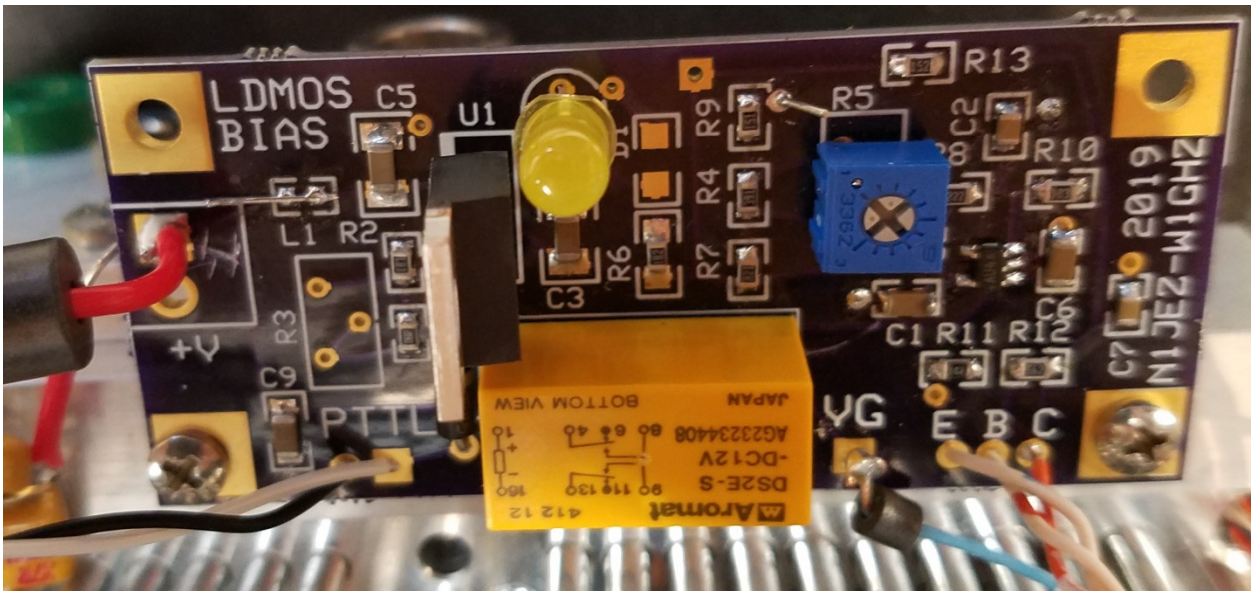

Figure 2 - LDMOS Bias Board Prototype mounted on amplifier

If anyone is interested, we can supply Gerber files for the PC board, which can be sent to OshPark (www.oshpark.com) to get 3 boards made at low cost. If there is sufficient interest, Paul might order a batch of PC boards.

LDMOS Bias Board

Parts List

Designator	8 volts	12 volts
C1	1uf	1uf
C2	0.1uF	0.1uF
C3	1uf	1uf
C5	0.1uF 100V	0.1uF 100V
C6	1uf	1uf
C7	0.1uF	0.1uF
C9	0.1uF	0.1uF
D1	LED	LED
L1	Ferrite Bead	Ferrite Bead
R2	180	180
R3	1K	1.5K
R3a	optional	optional
R4	390	390
R5	200 pot	200 pot
R6	1K	1.8K
R7	390	1K
R8	2.2K	2.2K
R9	75	75
R10	10K	10K
R11	1K	1K
R12	5.6K	5.6K
R13	1K	1.5K
Q1	2N3904	2N3904
U1	LM317AHV	LM317AHV
U2	LM7321MFX	LM7321MFX

Update 2020 – Dan, KW2T, points out that an LDMOS device should never have the gate floating with drain voltage on – "easiest way to blow up an LDMOS device."