FT-736R High Stability GPS Locked Reference
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Introduction

The Yeasu FT-736R is a VHF/UHF all mode radio. While it has not been sold for over 25+ years, a lot of them are still in use. They are still sought after. Mine covers 144/222/432/1296 MHz. It is one of the few rigs that will cover 222 MHz. As capable as it is, it was built before the rise of WSJT and other digital formats. I have used mine successfully on FT8, Q65 and Olivia with a SignaLink interface. However, its frequency accuracy/stability with some of the digital formats leaves much to be desired. The TCXO frequency reference in the 736 was state of the art in its day but some modes require more precise frequency setting and my 736 drifts 200-300 Hz on 1296 MHz during warm up. Its exact frequency is known only to about 100-200 Hz. Wouldn't it be nice if it could be be locked to a GPS disciplined reference? Even the owners of the more modern Icom 9700 have wished for this.

Frequency Synthesizer

The TCXO reference in the 736 is 20.48 MHz. This is the power of 2^{11} times 10 kHz. An eBay search turned up a voltage controlled 20.48 MHz crystal oscillator (VCXO) in a DIP can. (ebay item: 161185418304) It is still available as of 12/22. My GPS is a Trimble Thunderbolt that outputs 10 MHz. Could the 20.48 MHz VCXO be phase locked to 10 MHz?

The answer is yes and 80 kHz seems like a good comparison frequency. The 20.48 MHz divided by 256 yields 80 kHz. A divide by 256 requires two 4 bit dividers. A 74HC393 contains two 4 bit counters and it can be set up to divide by 256. The VCXO outputs a logic level so driving the counter should be easy. The 10 MHz from the GPS can be divided by 125 to get 80 kHz. The 125 divider requires three divide by 5's. These can be implemented in two 74HC390's. Figure 1 is a block diagram of the synthesizer.

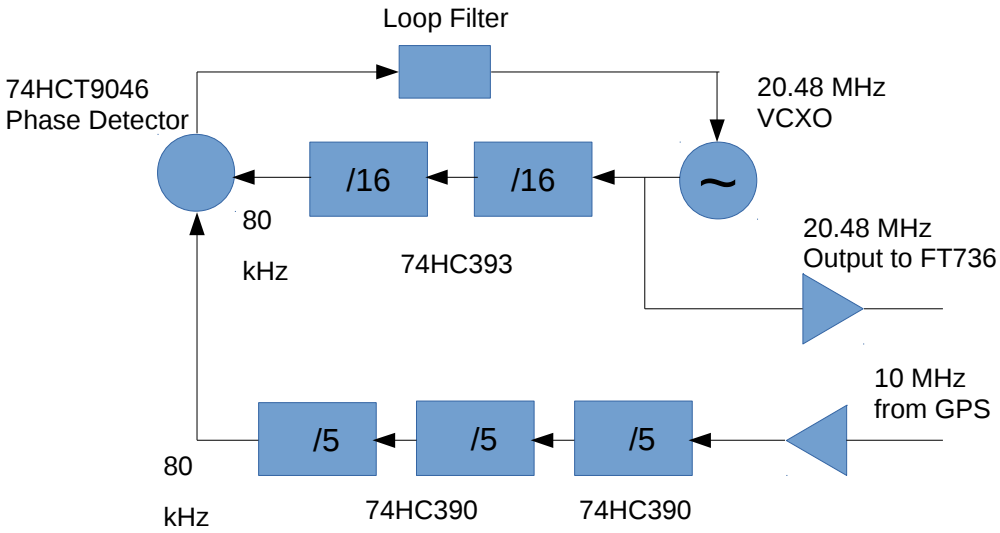


Figure 1: FT-736 GPS locked reference

The critical part of any phase locked loop (PLL) is the phase detector. A potential phase detector (PD) is the 74HC86 XOR gate. However, it has two limitations. First, it requires symmetric square wave inputs for correct operation. The divide by 256 will provide a square wave output but the divide by 125 does not. This could be overcome by using two of the unused divide by two's in the 74HC390's and doing the phase comparison at 40 kHz. The other problem with the 74HC86 PD is that it does not output a DC voltage but rather a pulse waveform at twice the reference frequency whose duty cycle is proportional to phase difference between the two signals. This requires careful filtering to suppress the spurious 80 kHz reference sidebands.

The 74HC4046 is a classic phase/frequency PD that does not suffer from these problems. It is edge triggered so the waveform duty cycle is unimportant and it outputs small relatively low energy correction pulses at lock that are easier to filter. However, its implementation produces a "dead zone" at zero phase error. The PLL effectively goes "open loop" at zero phase error. The resulting jitter will be multiplied up to 1296 MHz and it is unknown how problematic that would be. A more modern phase/frequency PD is the 74HCT9046. It has a true charge pump (switched current sources) output. Properly implemented, there is no dead zone and the loop filter acts like an active filter without the need for an op-amp. This part was originally made by Phillips, then NXP and then Nexperia. While it is still listed on Mouser's website, it is listed as obsolete. It is one of the few obsolete parts I would continue to use as there is no real replacement. Why does all the good stuff have to go obsolete? The SMT part does appear on eBay as does the DIP part. The DIP part is 74HCT9046AN. Check eBay, www.findchips.com or www.octopart.com for availability.

Synthesizer Circuit

Figure 2 is the schematic for the synthesizer. Q1 and U2C are an interface for the 10 MHz from the GPS. The required 10 MHz input is approximately 1V into 50 ohms. The interface circuit converts the input sine wave into a logic level waveform to drive the 74HC390. There is also a 10 MHz TCXO that can be configured for operation without the GPS. Pin 1 is jumpered to pin 2 on the "reference source" connector for the GPS input. Pin 2 is jumpered to pin 3 to use the TCXO as the reference. "TCXO pwr" connector is jumpered pin 1 to pin 2 for the GPS operation. That turns the TCXO off. Pin 2 jumpered to pin 3 applies 5V to TCXO. It is important to turn the TCXO off during GPS operation to prevent spurious outputs. R5 and R6 are the course and fine frequency trim for the TCXO. You need a TCXO with a frequency trim port.

A small 10 MHz oven controlled crystal oscillator (OCXO) might be an alternative to the 10 MHz TCXO. Find one that operates from 5V and has an HCMOS logic output. They are common on eBay but be aware they take considerably more current than the TCXO. Take the 12V power for the reference directly from the 12V power rail in the 736 and the LM7805 regulator will probably need a bigger heat sink.

U2A is a 20.48 MHz output buffer to the FT-736. C7, C8 and L1 form a low pass filter to convert the logic level output from U2A into a sine wave.

C11, C12 and R8 are the PLL loop filter. It is important to ground all the components associated with the feedback loop only in one place. This reduces the effect of ground loops. It is is difficult to get 70+ dB suppression of the reference sidebands without careful circuit layout. Pin 1 on U4 of the phase detector is grounded but it is returned with a short wire to the pin 1 ground on the VCXO. C12 also be connected to ground at the same point. Anyone who has worked with vacuum tube audio knows the art of single point grounding! It is the only way to keep the hum associated with the heater currents out of the low level stages.

The circuitry associated with U2D, U2F and U3 are a phase lock detector. While not formally required, it is a helpful indicator to tell you if everything is working. The 74HC74 will sink current so it can drive a small LED directly.

U4 is the phase detector. The 74HCT9046 is a complex part with a voltage controlled oscillator (VCO) and two different phase detectors. Phase detector PC2 is used for the phase lock. Its sensitivity is programmed with R12. The phase detector PC1 is used for the lock indicator circuit. The VCO is disabled by leaving pin 8 open.

12V is taken from the 736 to power the synthesizer. A LM7805 regulator on the synthesizer card provides 5V for the logic circuits. 0.01 uF bypass capacitors are used generously. The Vcc pin of each logic IC is bypassed.

Figure 3 is the measured performance of the PLL. The 80 kHz reference sidebands are suppressed to an unmeasurable level but there are 100 kHz spurs. The source of these spurs is unknown. They remain even when the PLL is disabled so they aren't the PLL. They are over 70 dB down and they do not appear to have any adverse effect..

Construction

Figure 4 and 5 show the construction of the GPS locked reference. The shielded box was made with 0.032" thick PCB material. It is important to have good shielding to keep the divider hash out of the radio. No interference has been detected.

The synthesizer was built on blank PCB material. A perf board with a 0.1"grid of holes was used as a template to drill patterns in the board for the DIP sockets. Use a couple small C claps to hold the board and the template in place. The perf board has 0.042" holes. Use a drill press and drill 0.042" (#58 drill). The holes can then be drilled out to 0.055" (#54 drill). When you are done drilling, clean the burr around around each hole by hand with another drill. So called "machined pin" DIP sockets should press into the holes with their pins coming fully through the board. Use an ohm meter to check that none of the pins are shorted to ground. Interconnections are made with #28 wirewrap wire. Strip a bit of the insulation off the end of a wire with a set of sharp wire cutters. Wrap the stripped end around a pin with a sharp object like a scriber and then solder the wire with a small iron. It takes some patience, practice and fine motor skills but I have successfully used this technique up to several hundred MHz with DIP parts.

Of course, if you are good at laying out PCB's, go for it. And share your design!

Interfacing with the FT-736

Figures 6, 7, 8 and 9 show the connection of the GPS locked reference to the 736. Connection is fairly straight forward. The only caveat that the TCXO in the 736 must be disabled. If left powered on, there is enough leakage to cause spurious outputs.

It was necessary to remove the circuit board the 736 in order to disable the TCXO and connect the reference. There are a lot of wires so exercise care. Be sure to disconnect the power before doing this. The PCB in the 736 is single sided phenolic and it is much more sensitive to heat damage than the fiberglass epoxy that we are used to.

Disclaimer

I have been using the GPS reference for well over a year and it works great however this is not a project for the inexperienced. It requires some disassembly of the 736 so be careful of what you do. Everyone's situation is different and I am not responsible if you damage your radio. Please, don't damage your radio!

BTW, I am told that the 736's PTT line goes directly into the computer and it is especially sensitive to damage from improper voltages. If you cook the computer, the radio is dead.

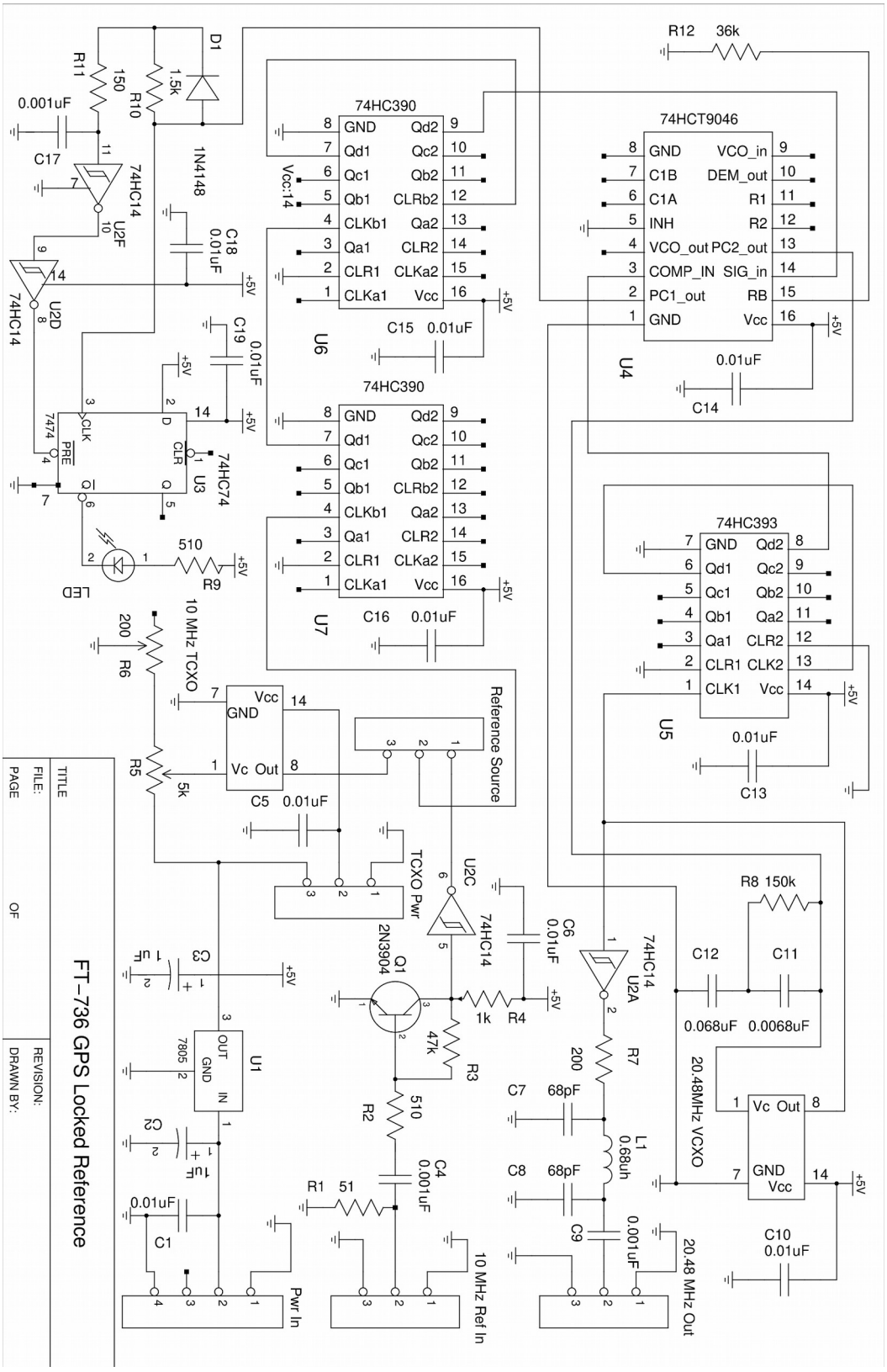


Figure 2: Schematic for the GPS locked reference.

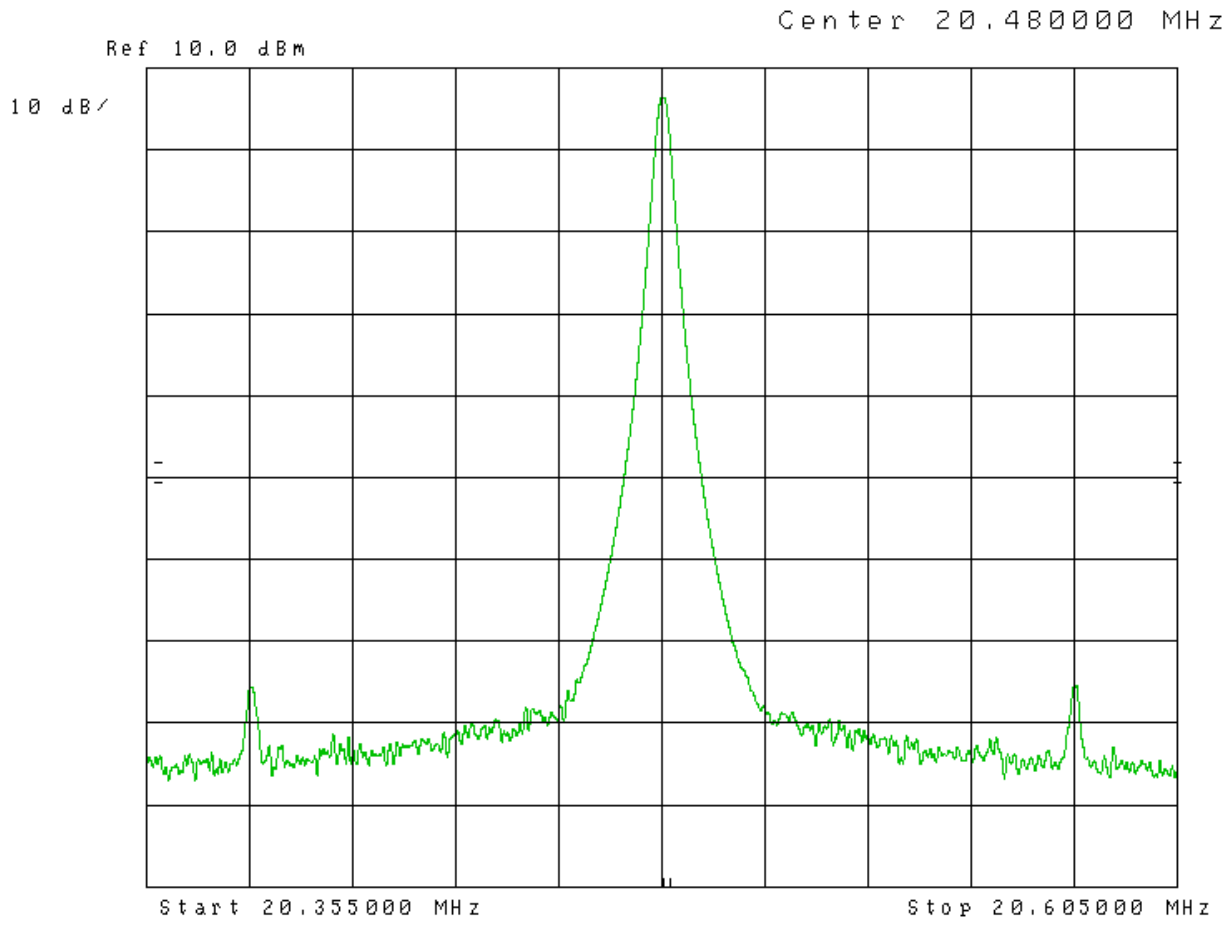


Figure 3: Reference output spectrum analyzer plot. Notice that there are no 80 kHz reference sidebands but there is a spurious at +/- 100 kHz. The source of this spurious is unknown. Is it coming out of the FT-736 on the 12V power? It is there even with the 10 MHz GPS turned off so it isn't the PLL. Since it is over 70 dB below the desired 20.48 MHz output it is not problematic.

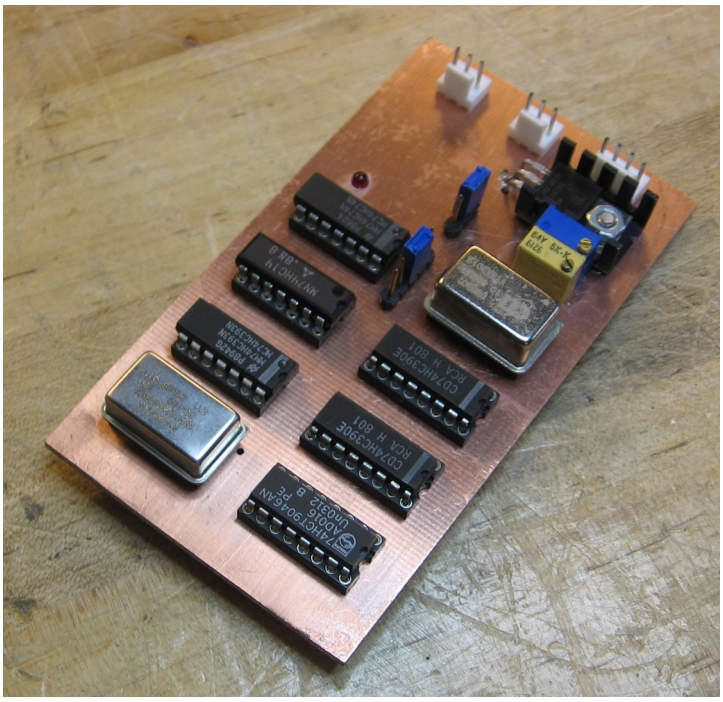


Figure 4: GPS locked reference. The 20.48 MHz VCXO is in the lower left. The oscillator can in the upper right is the 10 MHz TCXO. The two blue jumpers in the upper center connect the 10 MHz TCXO and allow operation without the GPS. The two pots above the TCXO set it on frequency and the lock LED is above the upper IC on the left.

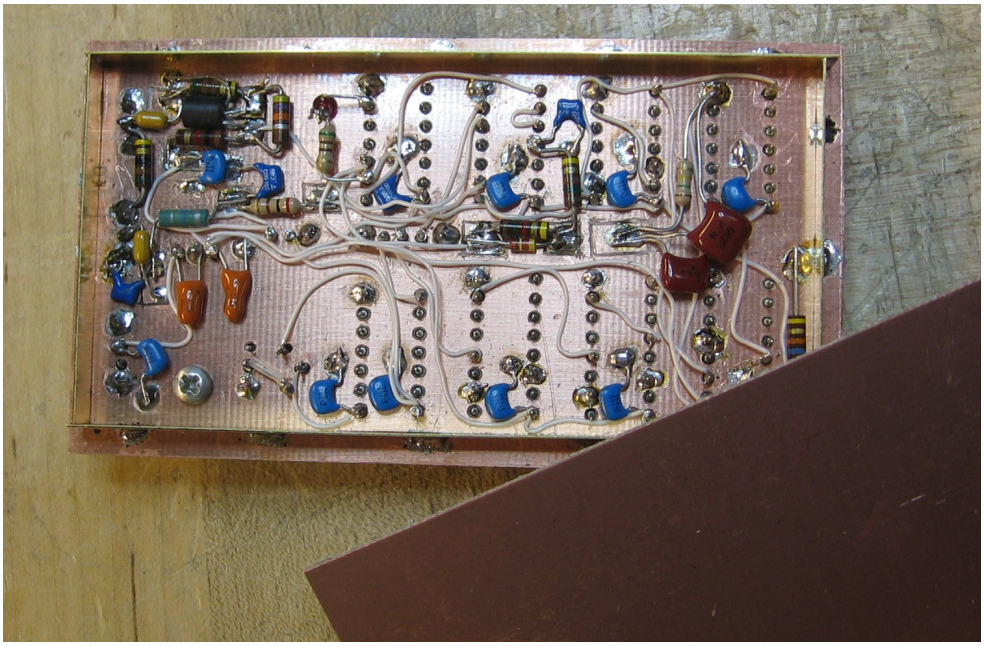


Figure 5: Interior of the reference. A small shielded box is formed with PCB material. The shielded enclosure is important to keep spurious signals from the synthesizer out of the radio.

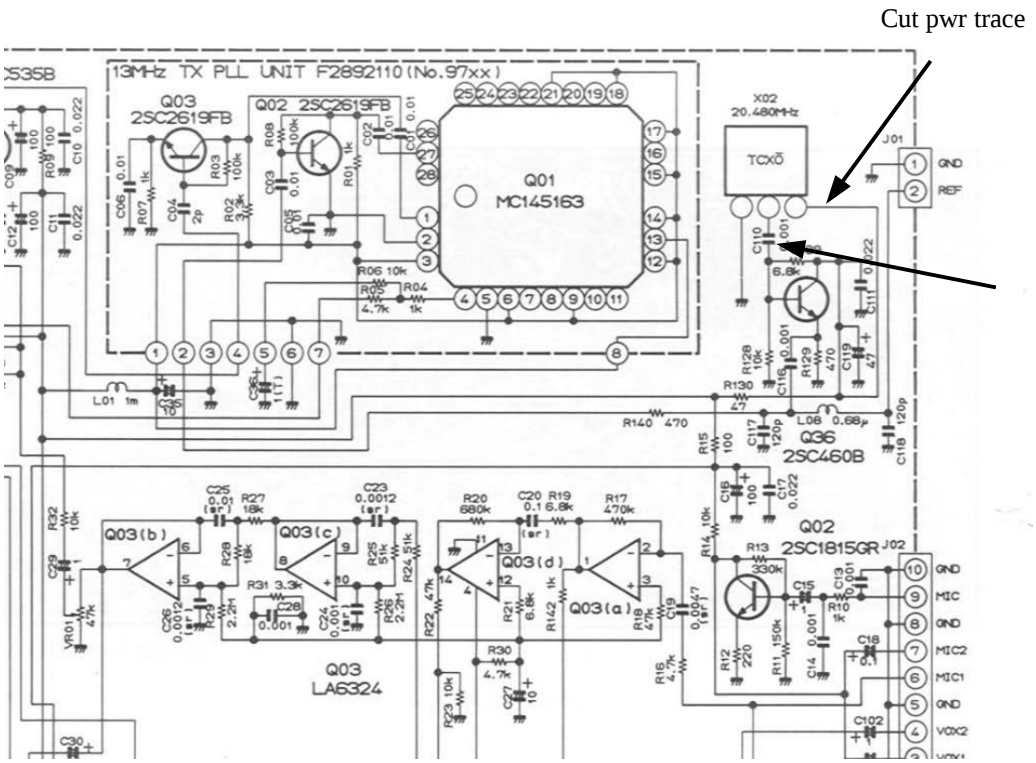


Figure 6: FT-736 schematic with TCXO reference. Disconnect the coupling capacitor C110. The end of C110 that went to the TCXO is connected to short length of co-ax to the new reference and ground the co-ax shield to the radio. It is also necessary to cut the power trace to the TCXO. If it is left running, the TCXO creates an undesirable spurious.

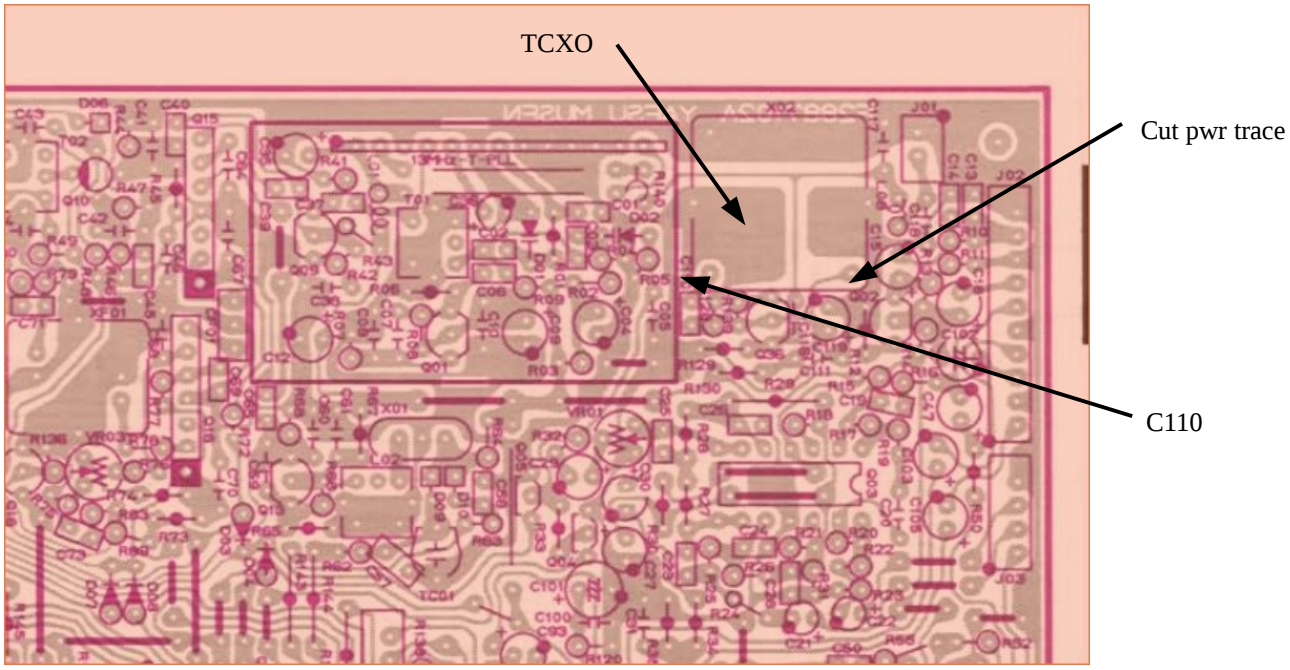


Figure 6: FT-736 board layout. You will have to remove the main 736 circuit board to make these modifications. Be careful, there are a lot of wires!

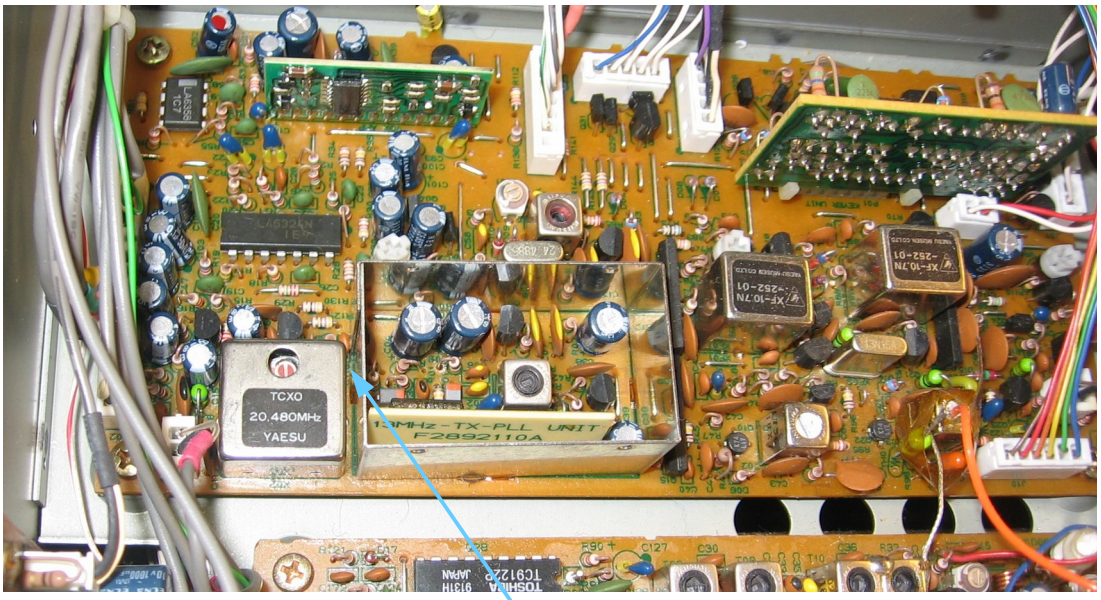


Figure 8: Interior of the FT-736 showing the TCXO.

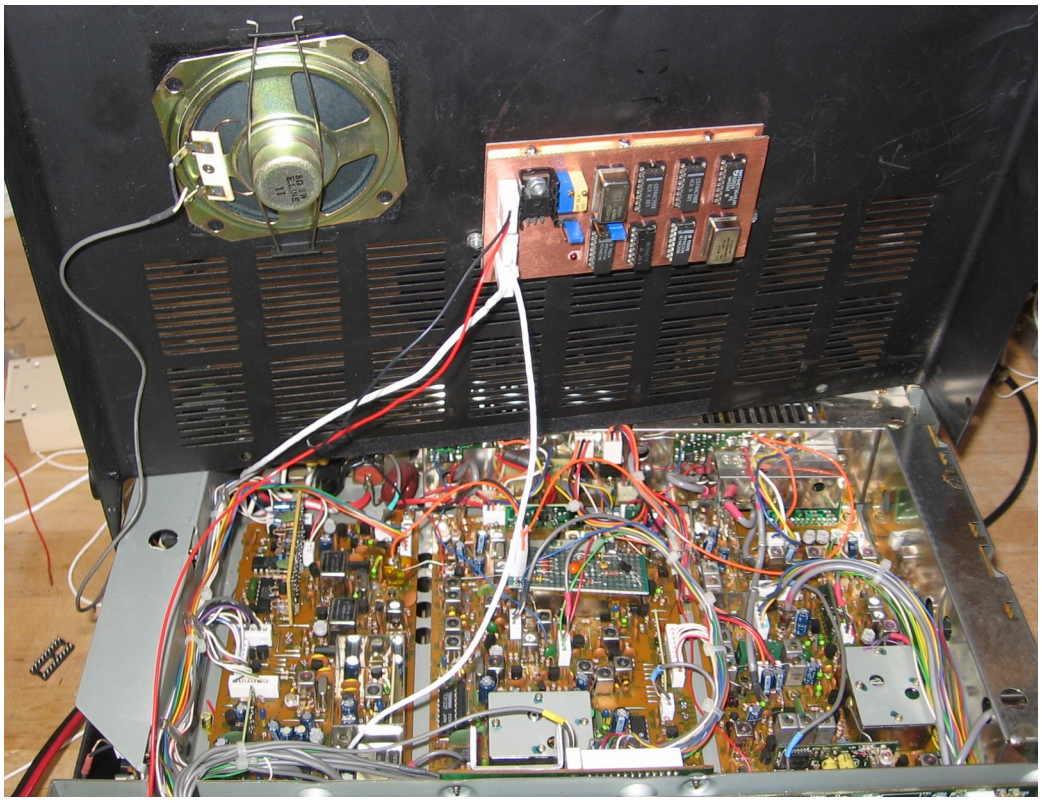


Figure 9: Reference installed on the cover of the FT-736. 12V power was taken from the transceiver to a LM7805 voltage regulator on the reference.

Appendix: PLL analysis

CMOS phase-locked loops: 74HC(T)4046A/7046A & 74HCT9046A, HCMOS Designer's Guide – advanced information, Revised edition: June 1995, Philips Semiconductors.

See p36

K_o = 1350 Hz/V measured tuning sensitivity of VCXO

K_n = 1/256 Divider ratio

K_p = 5/4π = 0.4V/rad Phase detector sensitivity

Set ω_n = 300 rad/s and ξ = 1.5

$$\omega_n = \sqrt{\frac{(K_p K_o K_n)}{\tau_1}} = 300 = \sqrt{\frac{((0.4)(2\pi)(1350)(1/256))}{\tau_1}}$$

$$\tau_1 = 147.3\,\mu sec$$

$$\zeta = \omega_n \frac{\tau_2}{2} = \frac{300}{2}\,\tau_2 = 1.5$$

$$\tau_2 = 10{,}000\,\mu sec$$

$R' = \tau_2 / C_2$ Choose C_2 = 0.068 μF $R' = \frac{(147.3\,E\,10^{-6})}{(0.068\,E\,10^{-6})} = 2166\,\Omega$

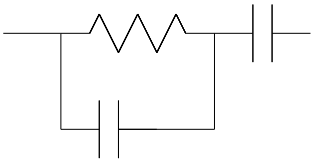
$R_{bias} = (2166)(17) = 36.8\,k = R12$ Use 36k

$R_4 = \frac{\tau_2}{C_2} = 0.01/(0.068\mathrm{E}10^{-6}) = 147\,K$ Use 150k

$\tau_3 = 0.1 = (0.1)(0.01) = (C_3)(R_4) = C_3(150\,k)$ C_3 = 0.0068 μF

R4
150k

C2
0.068 uF



C3
0.0068 uF

With ω_n = 300 rad/s and ξ = 1.5, the 3 dB BW of the PLL is:

$$BW_{3dB} = \omega_n\sqrt{\left(2\zeta^2+1+\sqrt{\left(2\zeta^2+1\right)^2+1}\right)} = 799.4\,rad/sec = 127.2\,Hz$$

Neither the bandwidth nor the damping are critical. While ξ = 1.5 is not optimum for transient response, it does result in a loop with a fairly flat response inside the loop BW. Low values of ξ result in a undesired peaking around ω_n.

K_o was measured. The loop can be adjusted for a different VCXO tuning sensitivity. Most VCXO's of this type will have a tuning sensitivity of 1000 – 1500 Hz /volt.