RADCOM TECHNICAL FEATURE

MSF Locked Frequency Reference

The first of a two part feature by Andy Talbot, G4JNT

WHEN OPERATING narrowband on the microwave bands, frequency setting can become a problem. Typically, crystal oscillators used in transverters can, with a certain amount of care, achieve 0.5 parts per million (ppm) accuracy when temperature compensation is used. However, at 10GHz this still corresponds to 5kHz uncertainty, nearly two SSB bandwidths! Frequency counters are available that can give accuracies of 1 part in 10^8 but these are expensive and not usually available when wanted.

Some years ago a frequency source based on the 200kHz long wave transmission from Droitwich was published. This suffered from residual phase modulation on the carrier and a good 'note' was difficult to obtain when multiplied to 10GHz. Since then, the Droitwich transmission has moved to 198kHz and the carrier is phase shift keyed at 25Hz during some times of the day, making a reliable and clean frequency standard much more difficult to achieve.

It was decided to adopt a different approach. The MSF Standard Frequency Transmission from Rugby on 60kHz is well known for transmitting time and date information which is easily decoded. The carrier frequency is related to International Standards, and is accurate to better than 1 in 10^{10}. This corresponds to an error at 10GHz of just 1Hz! In fact accuracy can be degraded by the transmission path at dusk and dawn, due to Doppler shift caused by the height of the Ionosphere changing, but this is unlikely to be noticeable.

It was decided to produce a general purpose frequency standard that had sufficiently good short term stability to be multiplied to microwave frequencies. In addition, lower frequencies would be provided that could be used as the timebase for frequency counters and oscilloscopes if required.

Direct multiplication of the 60kHz signal would not serve any useful purpose. No useful frequency could be produced for timebases, and the concept of directly multiplying by 172800 to 10GHz is mind boggling! In any case, the carrier is pulsed at 1Hz and an intermittent output would result.

The solution was to employ a 12MHz voltage controlled crystal oscillator which is divided down to 60kHz and phase locked to the MSF transmission. 12MHz was chosen for several reasons. Firstly, a simple to achieve division ratio of 200 gives the 60kHz VCXO signal. Secondly, all frequencies in the narrow-band segments of the microwave bands are (currently) multiples of 12MHz, making calibration simple. Since the prime purpose of the frequency standard was for calibrating my 10GHz equipment, a times-9 multiplier section was added to give a 108MHz output which could be used to generate a comb of harmonics detectable up to 10GHz.

The frequency reference is built in four modules, each one of which could be used for other purposes. A block diagram of the Reference is shown in **Fig 1**. The MSF signal is received off air by a ferrite rod antenna and head amplifier, mounted remotely. Any attempt to place the antenna near to the divider circuits will lead to pick up of the VCXO signal and the loop locking to itself rather than MSF. An NE567 tone decoder provides a gating signal corresponding to the carrier on/off keying. The received signal is squared up in an LM393 comparator, and applied to an Exclusive OR gate used as the phase detector for the PLL.

A 12MHz crystal oscillator is voltage tuned over a limited range of approximately 5ppm by the varicap across the crystal. The 12MHz output is applied to two bipolar tripler stages to give the 108MHz signal, and a portion is squared up and divided by 200 in a TTL divider chain. The resulting 60kHz output is applied to the other input of the phase comparator.

The output of the phase comparator has a mean level corresponding to the phase difference between the two signals when the carrier is on but settles to half output when the carrier is keyed off every second. The gating output of the tone decoder is used to control a sample-and-hold circuit consisting of a 4066 analogue switch and capacitor.

The voltage at this point is an accurate measure of the phase relationship between the two signals, and is displayed on a front panel meter to show the loop lock state. A loop filter integrates this output and uses it to control the VCXO frequency. Since a second order loop is used, the mean phase relationship is exactly 90° and the meter clearly shows when the loop is in lock by sitting firmly at mid scale.

An analogous system to this reference is used in colour television receivers to regenerate the colour subcarrier, at 4.43MHz, from a burst reference transmitted just after the line synchronising pulse. In this case the gating signal is generated by delaying the line

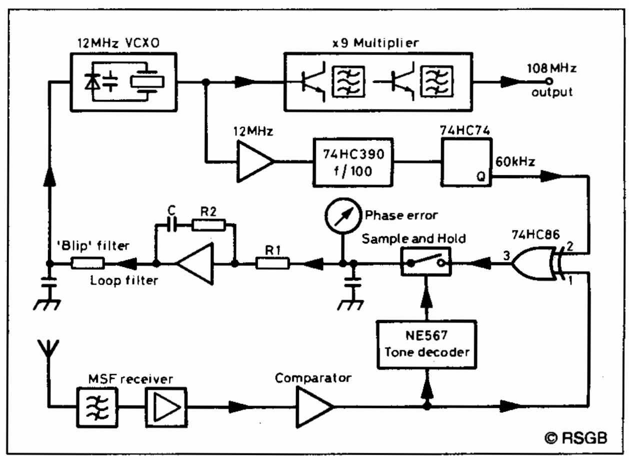


Fig 1: MSF Reference, block diagram.

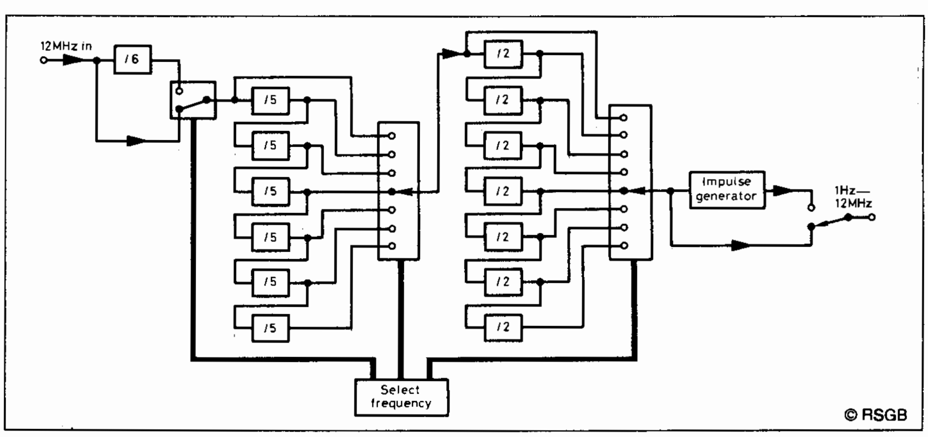


Fig 2: Programmable Frequency Divider, block diagram.

timebase flyback pulse.

To provide a range of other useful frequencies, a switchable, or programmable, divider is also included. The block diagram of this is shown in **Fig 2**. By selecting thumb-wheel switches, the 12MHz signal can be passed through between 0 to 7 divide-by-2 blocks, 0 to 6 divide-by-5 blocks and a possible divide-by-6. By this means 112 different frequencies down to 1Hz can be produced, by setting total division ratios from 1 to 12,000,000. All the 'useful' ones such as 1MHz, 25kHz etc can be obtained, as well as such frequencies as 93.75kHz and 375kHz. Who knows, they may be useful one day!

CONSTRUCTION

NO DETAILED CONSTRUCTION details are given as constructors will probably want to tailor the design to their own requirements. Separate units such as the times-9 multiplier and the programmable divider could be used on their own if desired.

The complete circuit diagram is given in **Figs 3, 4, 5 and 6**. The MSF head amplifier is built in a remote box and supplied with power via the coaxial cable. In spite of being at nearly audio frequencies, RF techniques need to be used here because of the low signal levels in this area. Input and output signals should be kept separate as the high gain in this block can easily cause oscillation. The ferrite rod antenna is a long wave unit, with extra capacitance added, and provides the only filtering needed. Bandwidth is around 1kHz, but depends to a large extent on the size of rod employed. The bigger the ferrite rod the larger the signal received.

The reference generator is made in three blocks. The VCXO and times-9 multiplier are on one board, which contains all the real RF circuitry. Layout should be suitable for the frequencies involved, and ideally a printed circuit board should be used. However, any other method of RF construction, such as the 'ugly' technique could be employed.

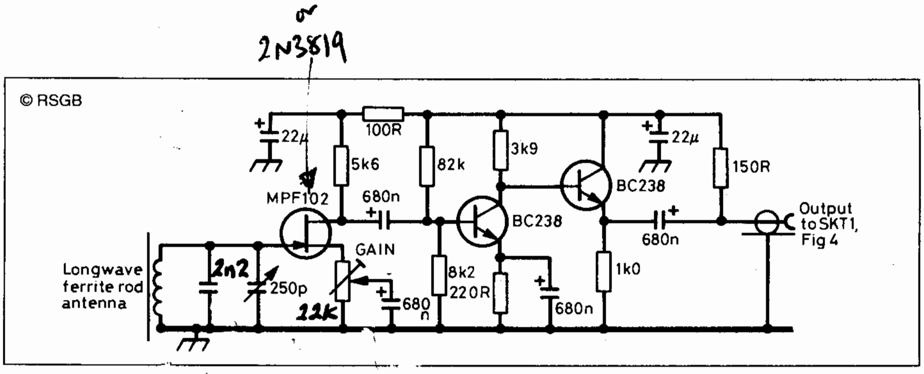


Fig 3: 60kHz Head Amplifier.

A second board contains all the sections needed for the PLL and the divide-by-200 circuitry, together with the MSF input comparator and tone decoder. Any 'logic' type construction such as point-to-point wiring is suitable. Care should be taken to keep the two 60kHz signals separate, as otherwise the loop will lock onto its own internally generated signal, and ignore MSF completely. Each integrated circuit should be by-passed with a 0.1μF capacitor at its pins, and ground connections should be as thick and direct as possible. If the 108MHz output is not required, the VCXO could also be incorporated on this board.

The same comments on decoupling and layout apply to the programmable divider; this should be kept away from the RF board as the low frequency signals could modulate the crystal oscillator in the event of any leakthrough.

ADJUSTMENTS

THERE ARE A NUMBER of adjustments to be set up and constructors are advised to follow the procedure given.

Firstly the VCXO is built and the 108MHz multiplier aligned. Monitor the voltage on the emitter of TR2 and peak L1 - L3 for a figure of 0.7V or higher. Then monitoring the emitter of TR3, peak L4 and L5. Finally, using a diode detector, peak L6 for maximum output. An output level of around 10dBm should be easily achieved, enough to drive a 1N23 type diode in a comb generator to 10mA.

The next stage is to bring the ferrite rod onto 60kHz. The use of an oscilloscope makes this a relatively straightforward job. With the head amplifier unpowered, connect the oscilloscope across the tuned circuit and, making sure the ferrite rod is at right angles to the direction of Rugby, adjust the preset capacitor until a 60kHz signal is seen which is pulsing on and off. Depending on the particular ferrite rod employed, it will probably be necessary to slide the coils along the rod to obtain resonance.

On the South Coast I am able to obtain a signal of 5 to 10mV peak-to-peak (p-p). If the head amplifier is now powered, a signal of more than 0.5V p-p sinewave should be present on the feeder. If a distorted signal much greater than this is present, the gain of the head amplifier should be reduced by adjusting the preset.

With the MSF signal applied to the Phase Locked Loop board, ensure that a 60kHz square-wave output from the LM393 comparator is present on pin 2 of the NE567. During breaks in carrier, noise should cause a random output at this point. Adjust the 10k preset until the LED flashes on and off with the received carrier. This completes the tone decoder setting up.

Set the lock / free switch so that the VCXO

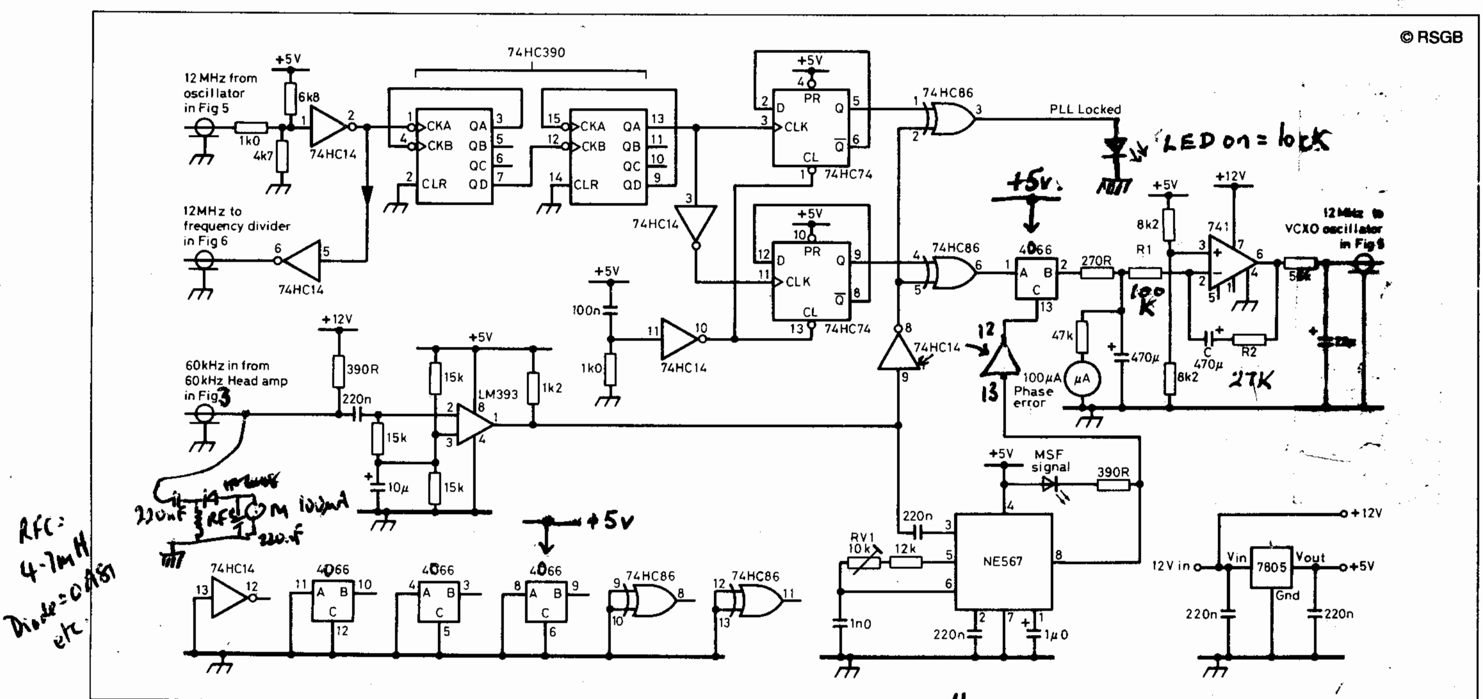


Fig 4: Comparator and part of Phase Locked Loop.

all IC voltage supplies bypassed with 0.1uF

Same with as phase error meter (switched)

See also Aug 94 Radcom p.64

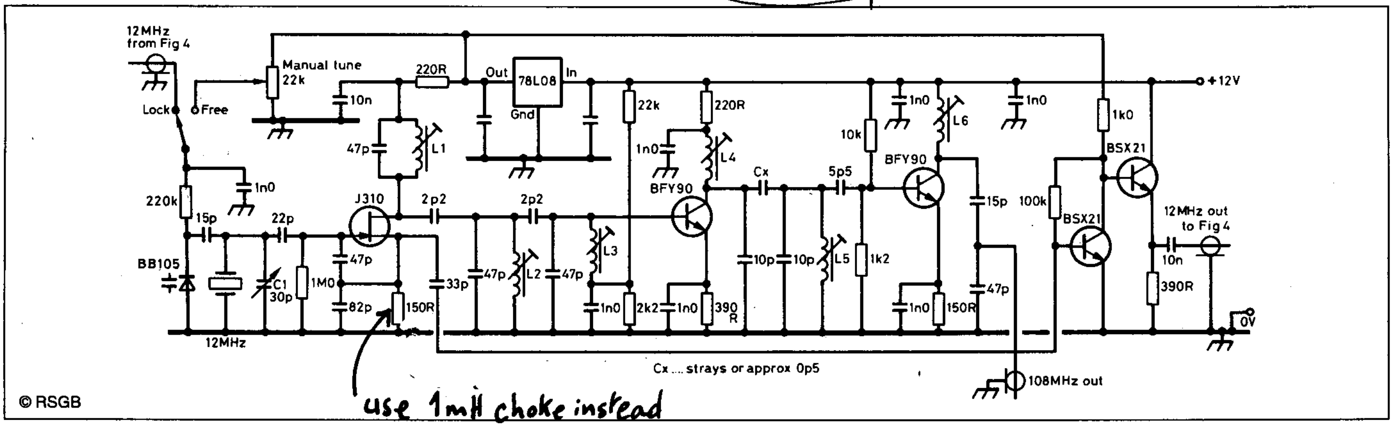
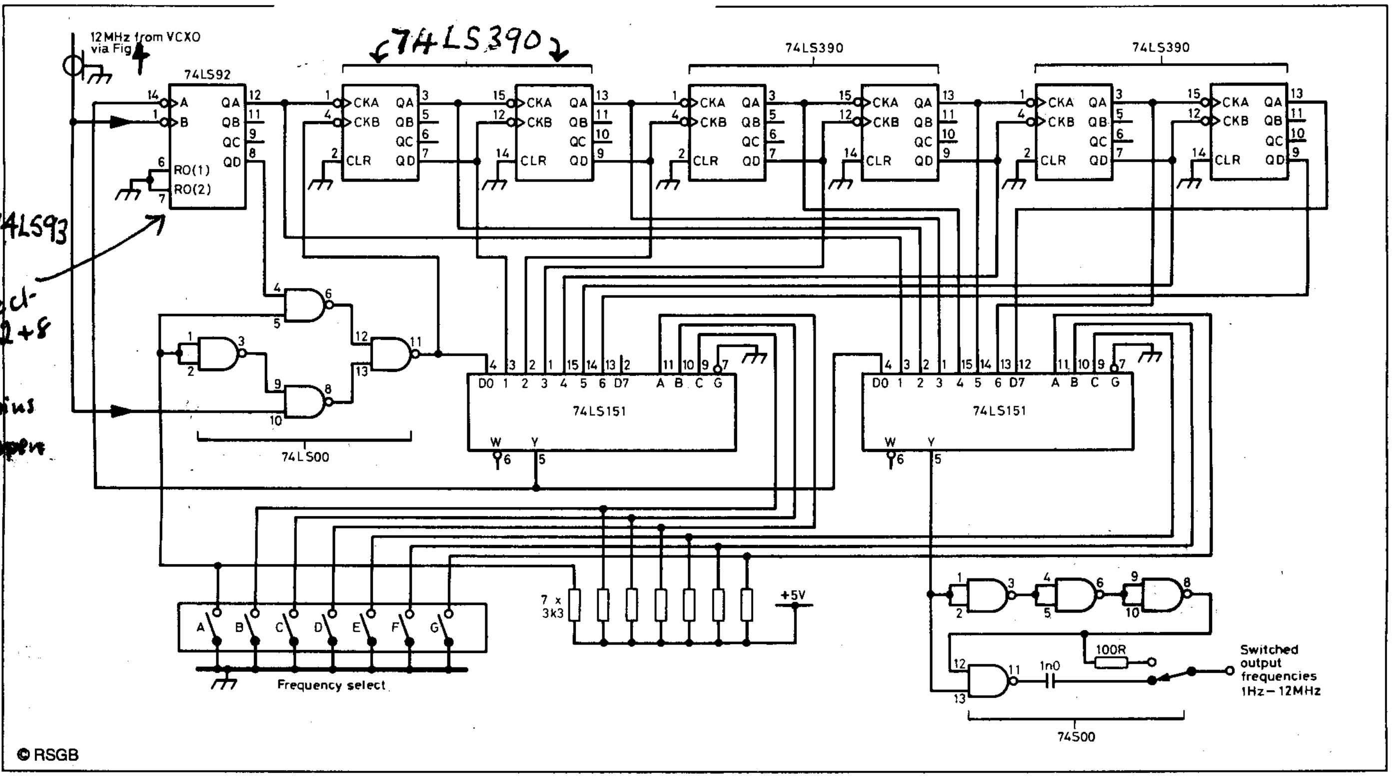


Fig 5: 12 MHz VCXO and Multiplier.



use 74LS93
Connect pins 2+8 3+11
leave pins 6+7 open

Fig 6: Switched Frequency Divider

free-runs and adjust VR1 for a VCXO tuning voltage of 3V. If the divide-by-200 circuitry is working correctly, the phase meter should now be swinging between 0 and FSD. If not, it is possible that the beat frequency between the VCXO and the received signal is too high for the meter to indicate.

Adjust the VCXO preset, C1, to bring this beat frequency as near as possible to zero. The error should be less than 0.1Hz, ie a complete cycle from zero to full scale and back to zero should take longer than ten seconds. Set the switch to Lock, discharge the 470µF capacitor, C1, by momentarily shorting it, and watch the meter. After three to four swings, the amplitude of the oscillation should have died away and the meter needle will be resting at mid scale, this is the 90° phase point and the loop is now locked.

If a digital voltmeter is available, monitor the tuning voltage over a period of one hour, it will drift due to the VCXO warming up, and if the voltage exceeds 3.5 Volts, C1 should be adjusted to achieve this value when locked. Harmonics of the VCXO can now be listened for on any band of choice and the calibration of receivers etc checked.

If at any point in the setting up, the MSF LED stays on, the receiver is picking up the internally generated 60kHz signal and the head unit should be moved further from the main unit. If all leads are sufficiently decoupled, a distance of 1 to 2 metres should be sufficient.

There is no setting up of the programmable divider, except by ensuring an output of the correct frequency is available for different settings of the programming switches.

. . . to be continued

NEXT MONTH

IN PART TWO, G4JNT will be detailing how to set up the receiver chain without using an oscilloscope.

RADCOM TECHNICAL FEATURE

MSF Locked Frequency Reference

The conclusion of a two part feature by A. C. Talbot, G4JNT

BY USING THE INTERNALLY generated 60kHz, it is possible to set up the receiver chain without using an oscilloscope.

Firstly, set up the tone decoder by feeding the 60kHz signal present at pin 9 of the 74HC74 to the MSF input. Adjust the 10k preset until the carrier LED lights. Now the tone decoder itself may be employed to set up the ferrite rod tuning. Adjust the preset capacitor and coil position until the LED is flashing reliably. In areas of low signal strength the phase meter could be used to maximise the received signal to noise ratio by adjusting for maximum deflection at the maxima and minima of the beat signal.

OPERATION

WHEN FIRST SWITCHING ON, with the loop set to 'lock', the meter will be observed to swing with a cycle time of a few seconds. After 3 to 4 swings, the amplitude will die away and the meter should sit at mid scale. If the two signals present at pins 1 and 2 of the 7486 are examined on a dual beam scope, no movement between them should be seen.

If the switch has been set to 'free' and the system free-running, then it may be difficult or impossible subsequently to achieve lock without switching the unit off and waiting for a few minutes. This is because, whilst free-running, the integrator output will probably have ramped up to its maximum of around 10 volts.

When the loop is subsequently closed, this voltage pulls the VCXO frequency outside the loop lock range and a beat frequency of 1Hz or so may be seen, the loop never being able to lock up to this frequency error. The quick solution is to discharge both 470μF capacitors so that they ramp up from zero towards the nominal tuning voltage of around 3V as if the unit had just been turned on.

One other problem that may occur is if the programmable divider (**Table 1**) is set to give an output where a close harmonic falls at 60kHz. (15, 20, 30kHz etc) In this case there is likely to be enough 60kHz leakage to cause the MSF signal to be overridden, and allow the loop to lock to itself. Should this occur, the carrier light will remain on and the VCXO frequency will either ramp to its maximum or minimum values. If left unchecked, it is possible that the tuning voltage could rise so high that subsequent lock cannot be achieved, in the same way as described above.

The 108MHz output should be sufficient to drive a 1N23 type microwave diode to 10mA or more diode current. This will give strong enough harmonics to be heard easily at 10GHz. At this frequency, on an SSB receiver, the received note is 'clean' but it is unlikely to be completely steady. A randomly varying change in the beat note of some 30 – 100Hz, over a period of several seconds, will probably be observed, due to several reasons. The primary one is the characteristics and signal to noise ratio of the MSF signal. Interference will perturb the loop operating point and cause a frequency variation whilst the loop tracks the signal. Another cause is instability in the VCXO. This random variation is actually phase noise, although it is difficult to think of noise as being at fractions of a Hz!

An interesting test is to warm the crystal by holding it whilst listening to the beat note. As the crystal warms up the frequency will quickly (within 1 – 2 seconds) drift. Over a longer period this will be corrected by the loop and the original beat return. Good construction techniques around the crystal oscillator will minimise this effect.

LOOP DESIGN

THE PHASE LOCKED LOOP has a very demanding specification. It has to reject totally the 1Hz component caused by the carrier pulsing. The sample and hold significantly reduces this component, but considerable 1Hz sidebands are still present. To achieve this, the loop bandwidth has to be significantly less than 0.5Hz and a figure of 0.12Hz was chosen. To calculate the values for the integrator time constants the characteristics of the VCXO and phase detector must be known. The VCXO constant (Kv), when divided down to 60kHz, was measured and a figure of 0.13Hz / volt obtained.

The phase detector figure can be calculated by assuming the output changes between the supply rails, ie from 0 to 5 volts, when the phase varies from 0 to 180°. Thus giving a phase detector constant of $5/\pi = 1.4$ volts / radian. A damping factor of 0.7 is used as giving an optimum compromise between loop tracking and lock up characteristics. The standard equations for phase locked loop lead-lag network time constants are employed:

$$t2 = \frac{2}{2\pi.BW} = 2.6\ \text{s}$$

$$t1 = \frac{(1 + KvKd.t2)^2}{4.2\pi.KvKd} \quad t2 = 3.56\ \text{s}$$

FREQ	X Y Z	FREQ	X Y Z	FREQ	X Y Z	FREQ	X Y Z
1.000	0 1 0	200.000	0 3 3	3.750k	1 5 0	62.500k	0 7 2
2.000	0 1 1	240.000	1 2 3	3.840k	1 2 7	75.000k	1 6 2
4.000	0 1 2	250.000	0 4 1	4.000k	0 4 5	80.000k	0 5 7
5.000	0 2 0	300.000	1 3 1	4.800k	1 3 5	93.750k	1 7 0
6.000	1 1 0	320.000	0 2 6	5.000k	0 5 3	96.000k	1 4 7
8.000	0 1 3	384.000	1 1 6	6.000k	1 4 3	100.000k	0 6 5
10.000	0 2 1	400.000	0 3 4	6.250k	0 6 1	120.000k	1 5 5
12.000	1 1 1	480.000	1 2 4	7.500k	1 5 1	125.000k	0 7 3
16.000	0 1 4	500.000	0 4 2	8.000k	0 4 6	150.000k	1 6 3
20.000	0 2 2	600.000	1 3 2	9.600k	1 3 6	187.500k	1 7 1
24.000	1 1 2	625.000	0 5 0	10.000k	0 5 4	200.000k	0 6 6
25.000	0 3 0	640.000	0 2 7	12.000k	1 4 4	240.000k	1 5 6
30.000	1 2 0	750.000	1 4 0	12.500k	0 6 2	250.000k	0 7 4
32.000	0 1 5	768.000	1 1 7	15.000k	1 5 2	300.000k	1 6 4
40.000	0 2 3	800.000	0 3 5	15.625k	0 7 0	375.000k	1 7 2
48.000	1 1 3	960.000	1 2 5	16.000k	0 4 7	400.000k	0 6 7
50.000	0 3 1	1000.000	0 4 3	18.750k	1 6 0	480.000k	1 5 7
60.000	1 2 1	1.200k	1 3 3	19.200k	1 3 7	500.000k	0 7 5
64.000	0 1 6	1.250k	0 5 1	20.000k	0 5 5	600.000k	1 6 5
80.000	0 2 4	1.500k	1 4 1	24.000k	1 4 5	750.000k	1 7 3
96.000	1 1 4	1.600k	0 3 6	25.000k	0 6 3	1000.000k	0 7 6
100.000	0 3 2	1.920k	1 2 6	30.000k	1 5 3	1.200M	1 6 6
120.000	1 2 2	2.000k	0 4 4	31.250k	0 7 1	1.500M	1 7 4
125.000	0 4 0	2.400k	1 3 4	37.500k	1 6 1	2.000M	0 7 7
128.000	0 1 7	2.500k	0 5 2	40.000k	0 5 6	2.400M	1 6 7
150.000	1 3 0	3.000k	1 4 2	48.000k	1 4 6	3.000M	1 7 5
160.000	0 2 5	3.125k	0 6 0	50.000k	0 6 4	6.000M	1 7 6
192.000	1 1 5	3.200k	0 3 7	60.000k	1 5 4	12.000M	1 7 7

X	Divide by 6 selector	Switch A
Y	Divide by 5 selector	Switches B,C,D
Z	Divide by 2 selector	Switches E,F,G

Table 1: Frequencies available from programmable divider.

Choosing a capacitor value of C = 470µF gives the necessary values of the resistors around the integrator to meet these time constants:

R1 = t1 / C R2 = t2 / C

Taking the nearest preferred values gives the values shown in the circuit diagram. A final network is added at the integrator output to give further attenuation at 1Hz. A time constant of 1.2s, formed by 56k and 22µF gives a further 19dB reduction in this component, whilst the time constant is fast enough not to affect the loop tracking performance. Without this extra filter, around 10Hz of frequency shift (at 10GHz) was noted every time the carrier was switched off. With the filter no shift was discernible.

CONCLUSIONS AND FURTHER MODIFICATIONS

THE FREQUENCY REFERENCE generated is more than good enough for 24GHz narrowband work in CW bandwidths! The unit has been designed so that different parts may be used separately as individual constructors wish. If other output frequencies are desired the following modifications could be made:

1) A 30MHz VCXO could be used instead of 12MHz, with a division ratio of 500 to give 60kHz. This would give access to 10MHz and 5MHz, not available from the unit described.
2) An output level of +10 dBm at 96MHz has been obtained from the multiplier, by changing the capacitors across the tuned circuits to give a quadrupler followed by a doubler stage.

There is further scope for optimising the loop feedback function. If the loop bandwidth could be narrowed still further, it would be less susceptible to noise and interference (but more so to oscillator stability). It would then probably be necessary to employ non-linear techniques to improve lock up time and pull in range.

If it is intended to use this unit portable, it may be necessary to temperature stabilise the crystal oscillator to prevent it moving outside the pull in range at temperature extremes. One way to do this would be to use the crystal heaters supplied by the RSGB's Microwave Component Service [Note 2].

NOTES

1 No components list has been provided as this article is intended as a source of ideas, rather than a perfectly reproducible construction project.

2 The RSGB Microwave Components Service can be contacted c/o Mrs P Suckling, G4KGC, 314A Newton Road, Rushden, Northants NN10 0SY; tel: 0933 411446.